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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,425	08/04/2000	Fabrice Geiger	A3024/T28300	1892

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APPLIED MATERIALS, INC.
2881 SCOTT BLVD. M/S 2061
SANTA CLARA, CA 95050

EXAMINER	
KILDAY, LISA A	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 12/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/632,425	GEIGER ET AL.	
	Examiner	Art Unit	
	Lisa A Kilday	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 10/29/02* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Election/Restrictions

This application contains claim 20 drawn to an invention nonelected with traverse in Paper No. 8. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Objections

Claim 19 is objected to because of the following informalities: "said porous silicon oxide layer" lacks antecedent basis. Appropriate correction is required.

Specification

The disclosure is objected to because of the following informalities: remove footnote on pg. 17.

In table 2, the value for the wet etch rate of bare silicon should be corrected to: 5,500 Å/min.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Cho (5,804,509).

In re claim 25, Cho discloses a method for forming an insulation layer over a substrate (1) having at least one gap (fig. 1) which is the area between each metal line (2), the method comprising: forming a surface sensitive silicon oxide layer (3) over the substrate (1) partially filling the at least one gap; and forming a porous silicon oxide

layer (4) on the surface sensitive silicon oxide layer by thermal CVD (col. 2 lines 53-55), wherein said porous silicon oxide layer is deposited at a temperature of about 400C or less (col. 2 lines 58-60).

In re claim 26, Cho discloses wherein the porous silicon oxide layer (4) fills the at least one gap (fig. 1A, col. 4 lines 62-65).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-2, 4-7, 9, 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (5,804,509) and Kwok et al. ("Surface related phenomena in Integrated PECVD/Ozone-TEOS SACVD Processes for sub-half micron gap fill: electrostatic effects", J. Electrochem. Soc., vol. 141, no. 8, Aug. 1994).

In re claim 1, Cho teaches a method for forming an insulation layer over a substrate, the method comprising: forming a surface sensitive silicon oxide layer (3) over the substrate (1); and forming a porous Silicon oxide layer (4) on the Surface sensitive silicon oxide layer (fig. 1) by thermal chemical vapor deposition, wherein said porous silicon oxide layer is deposited at a temperature of about 400C or less (col. 2 lines 50-60). However Cho does not teach wherein the porous silicon oxide layer has a wet etch rate of greater than about 6,000 Å/min. However, Kwok et al. teaches wherein the porous silicon oxide layer has a wet etch rate of greater than about 6,000 Å/min (pg. 2172 col. 2 lines 22-25, table IV, figs. 1-6). Therefore, it would be obvious to one skilled in the art at the time of the invention to form a porous silicon oxide layer with a wet etch

rate of greater than about 6,000 Å/min because it is well known in the art to deposit a porous Silicon oxide layer with an etch rate of 6,000 Å/min.

In re claim 2, Cho discloses the method of claim 1 wherein the porous silicon oxide layer has a carbon content of at least 5 atomic percent. It is inherent that an insulating film formed by a carbon containing silane, Tetraethylorthoxisilicate gas (TEOS), contains a carbon content of at least 5 atomic %.

In re claim 4, Kwok et al. teaches the method of claim 1 wherein the surface sensitive silicon oxide layer is deposited from a plasma enhanced CVD reaction of TEOS and oxygen (title, abstract, table IV).

In re claim 5, Cho teaches the method of claim 1 wherein the porous silicon oxide layer is deposited from a process gas comprising TEOS and ozone (col. 3 lines 53-60).

In re claim 6, Cho teaches the method of claim 5 wherein a molar ratio of said TEOS to ozone is between about 10:1 and 20:1 (col. 3 lines 7-15).

Claim 7 adds the limitation of forming a capping silicon oxide layer over the porous silicon oxide layer. Cho does not teach forming a capping layer over the porous silicon oxide layer. Kwok et al. teaches forming a capping layer over the porous silicon oxide layer (fig. 10). Therefore, it would be obvious to one skilled in the art to form a capping layer over the porous silicon oxide layer because in order to protect the porous silicon oxide during planarization.

In re claim 9, Cho teaches the method of claim 1 wherein said surface sensitive and porous silicon oxide layers are deposited in an in situ process (abstract lines 9-13).

In re claim 23, Cho teaches wherein the substrate (1) includes at least one gap (fig. 1), and wherein the surface sensitive silicon oxide layer (3) partially fills the at least one gap.

In re claim 24, Cho teaches wherein the substrate (1) includes at least one gap (fig. 1), and wherein the porous silicon oxide layer (4) partially fills the at least one gap.

Claims 3, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho and Kwok et al. as applied to claim 1 above, and in view of Lan (6,180,507).

In re claim 3, Cho teaches forming a surface sensitive silicon oxide layer over the substrate and a porous silicon oxide layer on the surface of the sensitive silicon oxide layer. Kwok et al. teaches wherein the porous silicon oxide layer has a wet etch rate of greater than about 6,000 Å/min (pg. 2172 col. 2 lines 22-25, table IV, figs. 1-6). However, neither Cho nor Kwok et al. teaches that the porous silicon oxide layer has a dielectric constant of between about 2.9 and 3.2. However, Lan teaches that the dielectric constant of porous silicon oxide layers are (208) between the dielectric constant of air 1.00059 and lower than the dielectric constant of a conventional silicon oxide layer, 4.0 (col. 3 lines 8-15). Therefore, it would be obvious to one skilled in the art to form a porous silicon oxide layer with a dielectric constant of between 2.9 and 3.2 because air in the holes of the porous silicon oxide layer reduce the dielectric constant in order to reduce RC delay. And, it would have been obvious to use silicon oxide with the etch rate of Kwok because it is well known in the art to deposit silicon oxide with an etch rate of 6,000 Å/min.

In re claim 8, Cho teaches the process of claim 1 wherein said porous silicon oxide layer is deposited. However, Cho does not teach using an SACVD process at a pressure of between 100-700 Torr. However, Lan teaches forming a porous silicon oxide layer (212) using TEOS and ozone at a pressure of 100-700 Torr (col. 2 lines 56-61). Therefore, it would be obvious to one skilled in the art to deposit porous silicon oxide layer at sub-atmospheric pressure in order for uniform and controlled deposition.

Claims 10-19, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho and Kwok in view of Lan.

In re claim 10, Cho teaches a method for depositing an intermetal dielectric film over a plurality of conductive lines (2). However, Cho does not teach depositing a plasma enhanced chemical vapor silicon oxide. Kwok teaches a method comprising: depositing a plasma enhanced chemical vapor deposition (CVD) silicon oxide layer (col. 2 lines 30-35, table II) over the plurality of conductive lines from a plasma of tetraethyloxysilane (TEOS) and oxygen (fig. 5); and depositing a silicon oxide layer over the plasma enhanced CVD silicon oxide layer by a thermal CVD process from a gas mixture of a TEOS and ozone (pg. 2174 col. 1 lines 15-20). Therefore, it would have been obvious to one of ordinary skill at the time of the invention to modify the process of Cho by depositing PECVD silicon oxide to reduce the stress hysteresis of the silicon oxide layer. However, neither Cho nor Kwok does not teach that said thermal silicon oxide layer has a dielectric constant of about 3.2 or less. It is inherent that an insulating film formed by a carbon containing silane, Tetraethylorthoxisilicate gas (TEOS), contains a carbon content of at least 5 atomic %. However, Lan teaches that

the dielectric constant of porous silicon oxide layers (208) are between the dielectric constant of air 1.00059 and lower than the dielectric constant of a conventional silicon oxide layer, 4.0 (col. 3 lines 8-15). Therefore, it would be obvious to one skilled in the art to form a porous silicon oxide layer with a dielectric constant of between 2.9 and 3.2 because air in the holes of the porous silicon oxide layer reduce the dielectric constant in order to reduce RC delay.

Claim 11 adds the limitation of wherein the density of said thermal silicon oxide layer is less than or equal to about 1.7 g/cm3. Cho teaches that the density of the thermal silicon oxide layer is less than or equal to about 1.7 g/cm3 (col. 5 lines 21-25).

Claim 12 adds the limitation of forming a PECVD silicon oxide layer capping over the thermal silicon oxide layer. Cho does not teach forming a capping layer over the thermal silicon oxide layer. However, Lan teaches forming a capping layer (214) over the thermal silicon oxide layer (208). Therefore, it would be obvious to one skilled in the art to form a capping layer over the thermal silicon oxide layer because the capping layer protects the thermal silicon oxide layer.

In re claim 13, Cho teaches forming a thermal silicon oxide layer. However, Cho does not teach that the dielectric constant of said thermal silicon oxide layer is greater than or equal to about 2.9. However, Lan teaches that the dielectric constant of porous silicon oxide layers are (208) between the dielectric constant of air 1.00059 and lower than the dielectric constant of a conventional silicon oxide layer, 4.0 (col. 3 lines 8-15). Therefore, it would be obvious to one skilled in the art to form a porous silicon oxide

layer with a dielectric constant that is greater than or equal to about 2.9 and 3.2 because air in the holes of the porous silicon oxide layer reduce the dielectric

Claims 14-16 adds the limitation of wherein a molar ratio of said TEOS and ozone used to deposit said thermal silicon oxide layer is at least 8:1. Cho teaches that a molar ratio of said TEOS and ozone used to deposit said thermal silicon oxide layer is at least 8:1 (col. 3 lines 7-15) and in the range of 10:1-20:1. However Cho does not teach the limitation of claim 10, wherein the thermal silicon oxide layer has a dielectric constant of about 3.2 or less. Lan teaches depositing a thermal oxide layer with TEOS and ozone with a dielectric constant that is lower than the conventional silicon oxide layer. It would be obvious to one skilled in the art to deposit a thermal silicon oxide layer with a molar ratio of TEOS to O3 that is greater than 8:1 but in the range of 10:1 and 20:1 as a matter of routine optimization.

Claim 17 adds the limitation of wherein said oxygen is provided from a flow of molecular oxygen. Cho does not teach providing a molecular oxygen source. However, Lan teaches forming a thermal CVD layer using a molecular oxygen source as a source of oxygen (col. 2 lines 56-60). It is well known in the art to use molecular oxygen as the source of oxygen. Therefore, it would be obvious to one skilled in the art to deposit a thermal silicon oxide layer using molecular oxygen as a source for oxygen in addition to TEOS or ozone because molecular oxygen is an inexpensive source of oxygen and well-known substitute for O3 or TEOS.

Claim 18 adds the limitation of wherein said plasma enhanced and thermal CVD silicon oxide layers are deposited in an in situ process. Kwok teaches forming PECVD

and thermal CVD silicon oxide layers in situ (abstract lines, title, pg. 2172 lines 40-50). However, Kwok does not teach forming a low dielectric constant layer. However Lan teaches forming CVD layers that have a low dielectric constant layer. It is well known in the art to form silicon oxide layers in situ. Therefore, it would be obvious to one skilled in the art to form PECVD and thermal silicon oxide layers in situ as taught by Kwok et al. in order to reduce the dielectric constant as taught by Lan.

In re claim 19, Cho teaches the process of claim 10 wherein said porous silicon oxide layer is deposited. However, Cho does not teach using an SACVD process at a pressure of between 100-700 Torr. However, Lan teaches forming a porous silicon oxide layer (212) using TEOS and ozone at a pressure of 100-700 Torr (col. 2 lines 56-61). Therefore, it would be obvious to one skilled in the art to deposit porous silicon oxide layer at sub-atmospheric pressure in order for uniform and controlled deposition.

In re claim 21, Cho does not teach wherein the plasma enhanced CVD silicon oxide layer partially fills gaps between the plurality of conductive lines. However, Kwok teaches forming plasma enhanced CVD silicon oxide (abstract) to partially fills gaps between the plurality of conductive lines (pg. 2172 col. 1 lines 14-25). Therefore it would be obvious to one skilled in the art to form plasma enhanced CVD silicon oxide to partially fills gaps between the plurality of conductive lines in order to promote gap fill capability.

In re claim 22, Cho does not teach wherein the thermal silicon oxide layer partially fills gaps between the plurality of conductive lines. However, Lan teaches forming thermal silicon oxide (212) to partially fill gaps between the plurality of

conductive lines (fig. 2E, col. 3 lines 39-41). Therefore it would be obvious to one skilled in the art to form thermal silicon oxide to partially fills gaps between the plurality of conductive lines in order to prevent cross talk between metal lines to improve quality of the devices.

Response to Arguments

Applicant's arguments filed 10/29/02 have been fully considered but they are not persuasive.

Claim Objections:

Applicant failed to address the claim objection of claim 19 and make appropriate corrections to claim 19 in their amendment. "Said porous silicon oxide layer" lacks antecedent basis. Claim 19 is dependent on independent claim 10, which does not recite "porous silicon oxide layer". It is unclear whether "said porous silicon oxide layer" is drawn to the "plasma enhanced CVD silicon oxide layer" or "thermal silicon oxide" in claim 10. Appropriate correction to claim 19 is required.

Specification:

Applicant failed to address the objection to the disclosure. Applicant needs to remove the footnote found on pg. 17.

Election/Restriction:

Applicant's election with traverse of method for forming an insulation layer in Paper No. 12 is acknowledged. The traversal is on the ground(s) that the apparatus of claim 20 is not materially distinct from the process claims 1-19 because the apparatus claims encompass any and every computer implementation of the process recited in the

process claims. This is not found persuasive because the process of claims 1-19 do not need the computer-readable program found in the system of claim 20 because the human mind can be used instead of a computer-readable program to form an insulation layer of claims 1-19.

The requirement is still deemed proper and is therefore made FINAL.

Nevertheless, upon allowance of any of claims 1-19, claim 20 will be rejoined and allowed with that claim, if it includes all the limitations of that claim.

Cho teaches in fig. 1A forming a porous silicon oxide layer (4) on the surface sensitive silicon oxide layer (3). Cho does not teach wherein porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min. However, Kwok teaches forming a porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min. Due to the amendment, claims 1, 2, 4-6, 9 are rejected under 103.

The method of Cho of forming an insulating film by a carbon containing silane, TEOS, which inherently contains a carbon content of at least 5 atomic %.

Claims 3, 8, 10-19 are unpatentable over Cho and Kwok et al. in view of Lan. Lan teaches that the dielectric constant of porous silicon oxide layer is lower than that of conventional silicon oxide (col. 3 lines 8-15). Lan's layer –208- of porous silicon oxide is a dielectric layer. The porous silicon oxide layer contains air; the air holes are what make this layer (208) porous. The dielectric constant of a conventional silicon oxide layer is 4.0 – 4.9. The dielectric constant of air is 1.00059. The dielectric constant of porous silicon oxide is in the range of 1.00059 – 4.0. Therefore, the dielectric constant of porous silicon oxide is taught to be on the claimed layer.

Lan teaches forming a porous silicon oxide layer (212). Lan teaches that the porous silicon oxide layer (212) consists of two portions: a porous silicon oxide (208) and a dense silicon oxide (210) (col. 2 lines 62-64). Therefore it would be obvious to one skilled in the art to form different types of silicon oxide due to different bonding situations (col. 3 lines 1-7). Cho teaches forming a porous silicon oxide layer (4) on a surface sensitive oxide layer (3). Kwok et al. teaches wherein the porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min. Furthermore, applicant is aware that this etch rate is well known because the Applicant's Admitted Prior Art (APA) teaches that a porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min is well known in the art. See pg. 17 lines 13-19, table 2. Cho has the benefit of a preferred method, which fills the gaps with homogenous step coverage and prevents voids due to the penetration of moisture (col. 1 lines 50-54).

Cho and Lan do not teach depositing a plasma enhanced CVD layer. However, Kwok teaches a the method comprising: depositing a plasma enhanced chemical vapor deposition (CVD) silicon oxide layer (col. 2 lines 30-35, table II) over the plurality of conductive lines from a plasma of tetraethyloxysilane (TEOS) and oxygen (fig. 5); and depositing a silicon oxide layer over the plasma enhanced CVD silicon oxide layer by a thermal CVD process from a gas mixture of a TEOS and ozone (pg. 2174 col. 1 lines 15-20). Lan discloses that the thermal silicon oxide layer has a dielectric constant of about 3.2 or less. Lan teaches that the dielectric constant of porous silicon oxide layers are (208) between the dielectric constant of air 1.00059 and lower than the dielectric constant of a conventional silicon oxide layer, 4.0 (col. 3 lines 8-15). The dielectric

constant depends on the degree of porosity of the layer. Cho discloses a porous silicon oxide layer by forming it with TEOS. It is inherent that an insulating film formed by a carbon containing silane, Tetraethylorthoxisilicate gas (TEOS), contains a carbon content of at least 5 atomic %.

Neither Cho nor Lan disclose forming plasma enhanced CVD layers. However, Kwok teaches forming CVD layers with plasma (title, abstract, pg. 2172 col. 1 lines 10-15). Therefore it would be obvious to one of ordinary skill at the time of invention to modify the process of either Cho or Lan by forming plasma enhanced CVD layers as taught by Kwok in order to form a very porous film with a low dielectric constant and higher etch rate.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0957. See MPEP 203.08.

Any inquiry concerning this communication from the examiner should be directed to Lisa Kilday whose telephone number is (703) 306-5728. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on (703) 308-1233. The fax number for the group is (703) 305-3432. MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

Lisa Kilday

LAK

12/9/02

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800